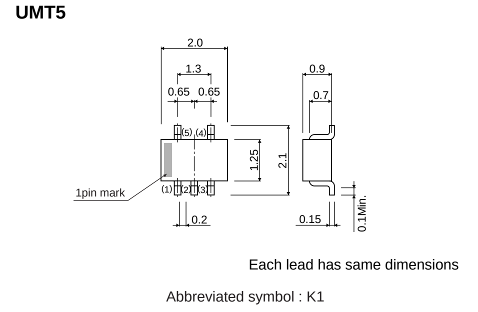
2.5V Drive Nch+Nch MOS FET

UM5K1N

●Structure
Silicon N-channel MOS FET

●External dimensions (Unit : mm)



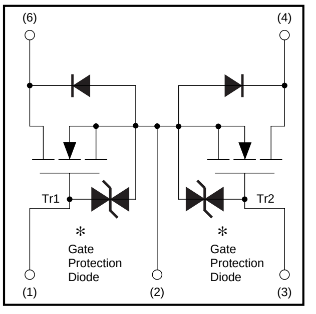
●Features
1) Two 2SK3018 transistors in a single UMT package.
2) Mounting cost and area can be cut in half.
3) Low on-resistance.
4) Low voltage drive (2.5V) makes this device ideal for portable equipment.
5) Drive circuits can be simple.

●Applications
Interfacing, switching (30V, 100mA)

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
UM5K1N		○

●Equivalent circui



(1) Tr1 Gate
(2) Source
(3) Tr2 Gate
(4) Tr2 Drain
(6) Tr1 Drain

∗ A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltagesare exceeded.

●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±100	mA
	Pulsed	I_{DP} ∗1	±400	mA
Total power dissipation		P_D ∗2	150	mW / TOTAL
			120	mW / ELEMENT
Channel temperature		Tch	150	˚C
Storage temperature		Tstg	–55 to +150	˚C

∗1 Pw≤10µs, Duty cycle≤50%
∗2 With each pin mounted on the recommended lands.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	833	°C / W / TOTAL
		1042	°C / W / ELEMENT

∗ With each pin mounted on the recommended lands.

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-source leakage	I_{GSS}	–	–	±1	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	0.8	–	1.5	V	V_{DS}=3V, I_D=100μA
Static drain-source on-stage resistance	$R_{DS(on)}$	–	5	8	Ω	I_D=10mA, V_{GS}=4V
	$R_{DS(on)}$	–	7	13	Ω	I_D=1mA, V_{GS}=2.5V
Forward transfer admittance	$\lvert Y_{fs} \rvert$	20	–	–	mS	I_D=10mA, V_{DS}=3V
Input capacitance	C_{iss}	–	13	–	pF	V_{DS}=5V
Output capacitance	C_{oss}	–	9	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	4	–	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$	–	15	–	ns	I_D=10mA, V_{DD}≒5V
Rise time	t_r	–	35	–	ns	V_{GS}=5V
Turn-off delay time	$t_{d(off)}$	–	80	–	ns	R_L=500Ω
Fall time	t_f	–	80	–	ns	R_G=10Ω

●Electrical characteristic curves

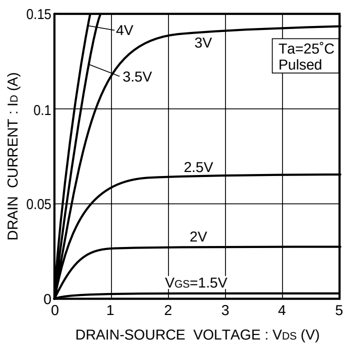


Fig.1 Typical output characteristics

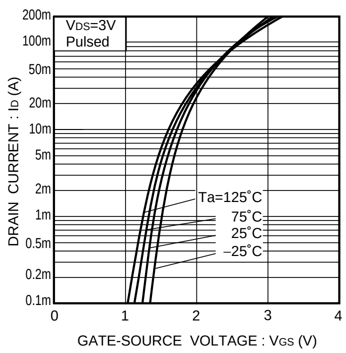


Fig.2 Typical transfer characteristics

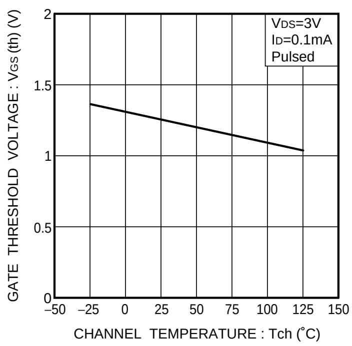


Fig.3 Gate threshold voltage vs. channel temperature

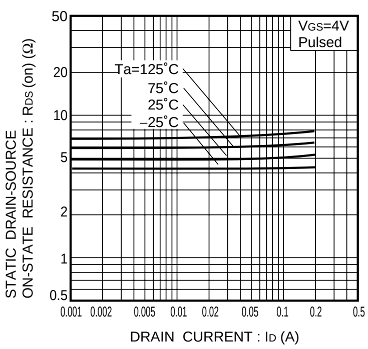


Fig.4 Static drain-source on-state resistance vs. drain current (I)

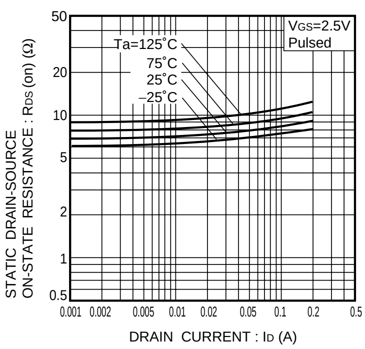


Fig.5 Static drain-source on-state resistance vs. drain current (II)

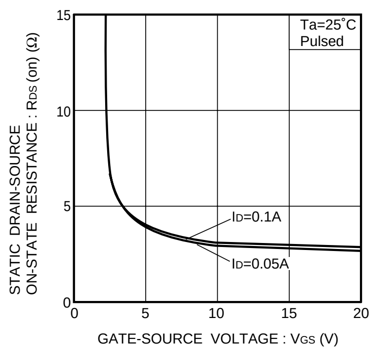


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

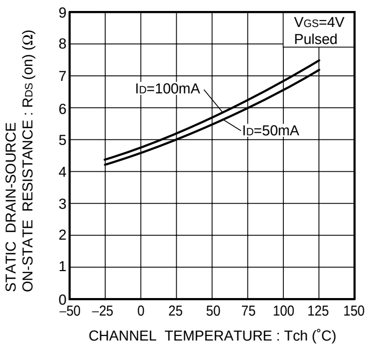


Fig.7 Static drain-source on-state resistance vs. channel temperature

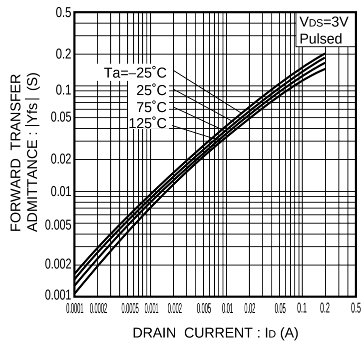


Fig.8 Forward transfer admittance vs. drain current

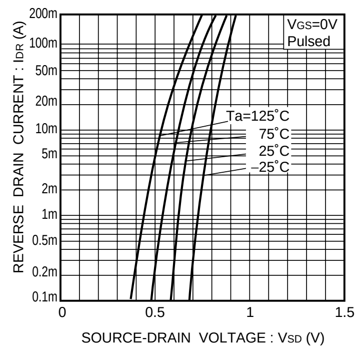


Fig.9 Reverse drain current vs. source-drain voltage (I)

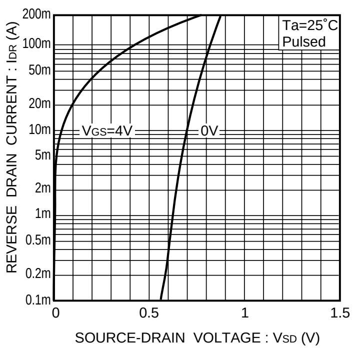


Fig.10 Reverse drain current vs. source-drain voltage (II)

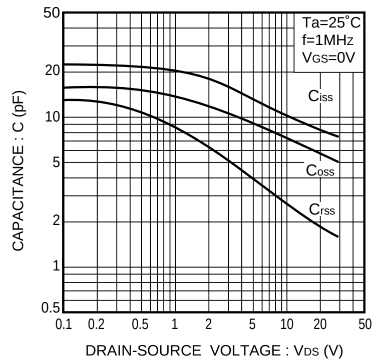


Fig.11 Typical capacitance vs. drain-source voltage

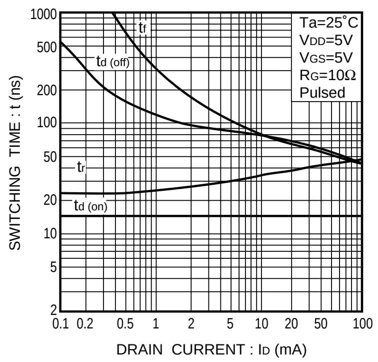


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurment circuit and resultant waveforms)

●Switching characteristics measurement circuit

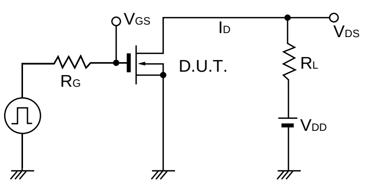


Fig.13 Switching time measurement circuit

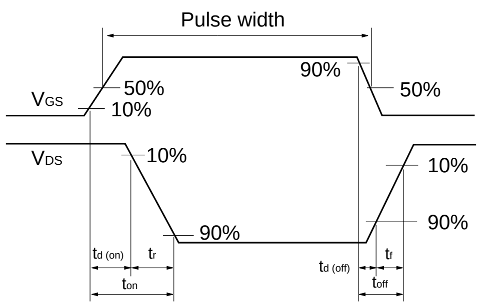


Fig.14 Switching time waveforms

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